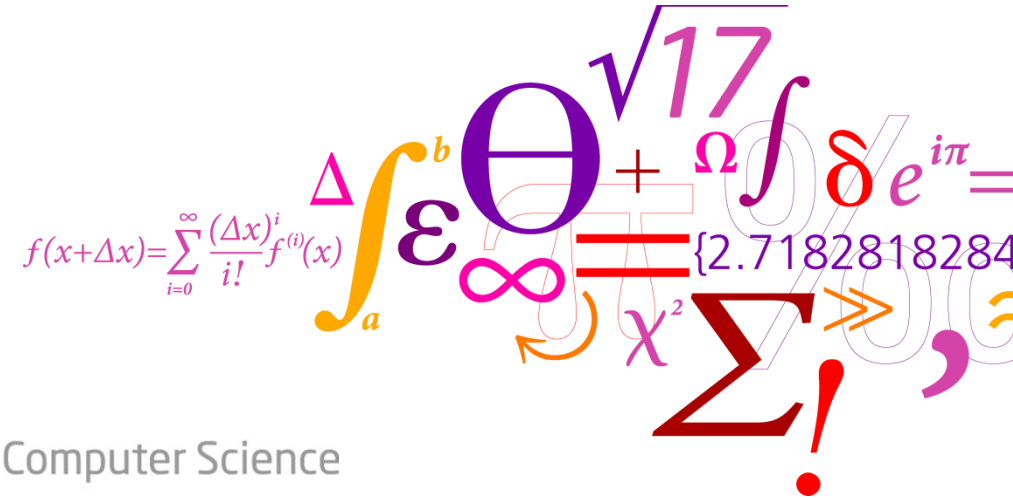
A Time-predictable TTEthernet Node

Maja Lund, Luca Pezzarossa, Jens Sparsø, and Martin Schoeberl



DTU Compute
Department of Applied Mathematics and Computer Science

Overview

- Distributed real-time systems
  - Set of real-time computing systems
  - Communication fabric
- Deterministic networks
  - TTCAN, Flexray, etc.
  - EtherCAT, Ethernet Powerlink, TSN, TTEthernet
- Time-predictable TTEthernet node based on the Patmos processor
  - Open-source
  - No proprietary hardware in the node

Outline

1) Background on TTEthernet

2) Our TTEthernet node

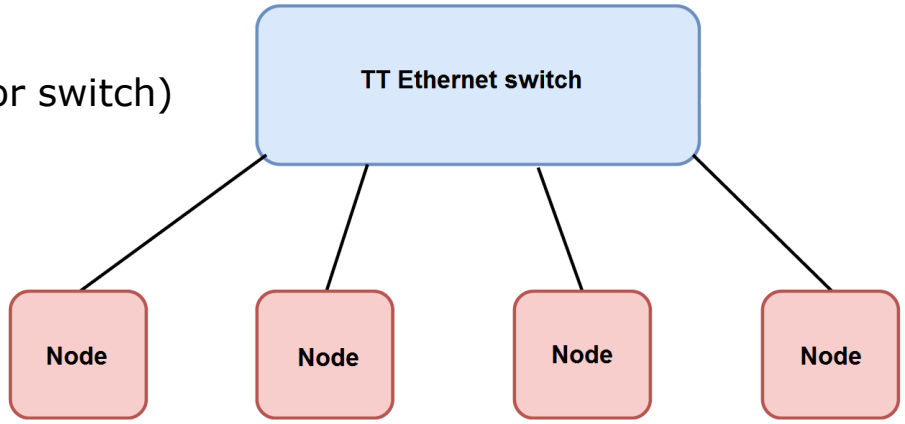
3) Functionality

4) Evaluation

5) Summary

Background on TTEthernet

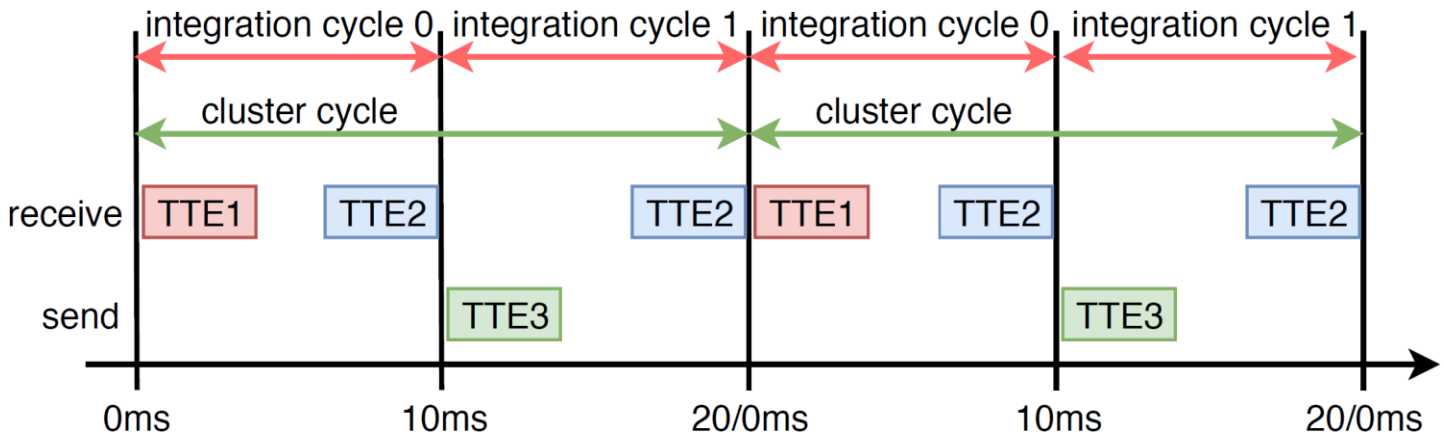
- Time-triggered Ethernet
- Deterministic extension of Ethernet (OSI data link layer)
  - Best effort traffic
  - Critical traffic: rate-constrained and time-triggered
- Time-triggered traffic
  - Virtual links between nodes
  - Static schedule (for nodes and for switch)
  - Switch enforce the schedule



Background on TTEthernet

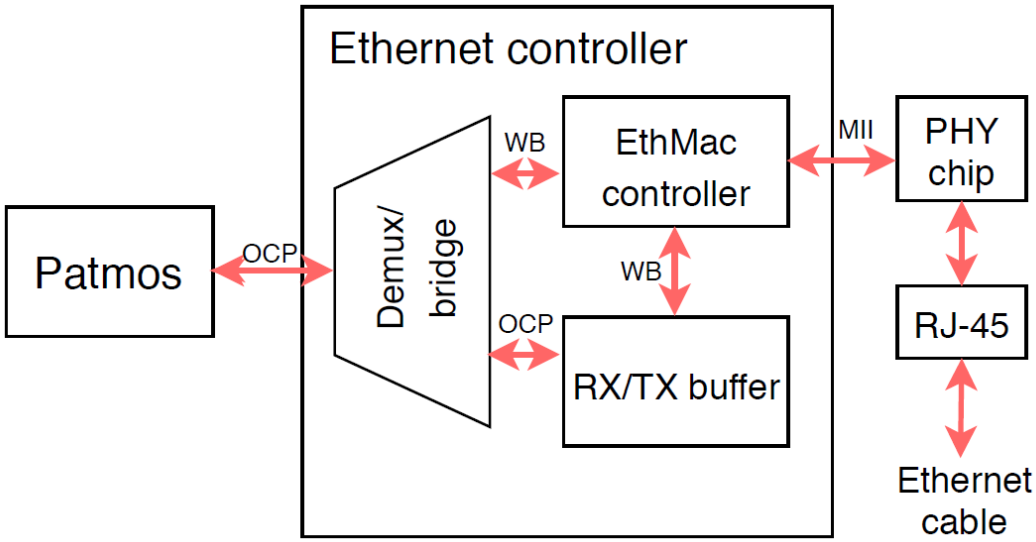
- Global notion of time
  - Periodic synchronization (integration cycle)
  - Periodic schedule (cluster cycle)

- Synchronization using protocol control frames from sync-master



Our TTEthernet Node

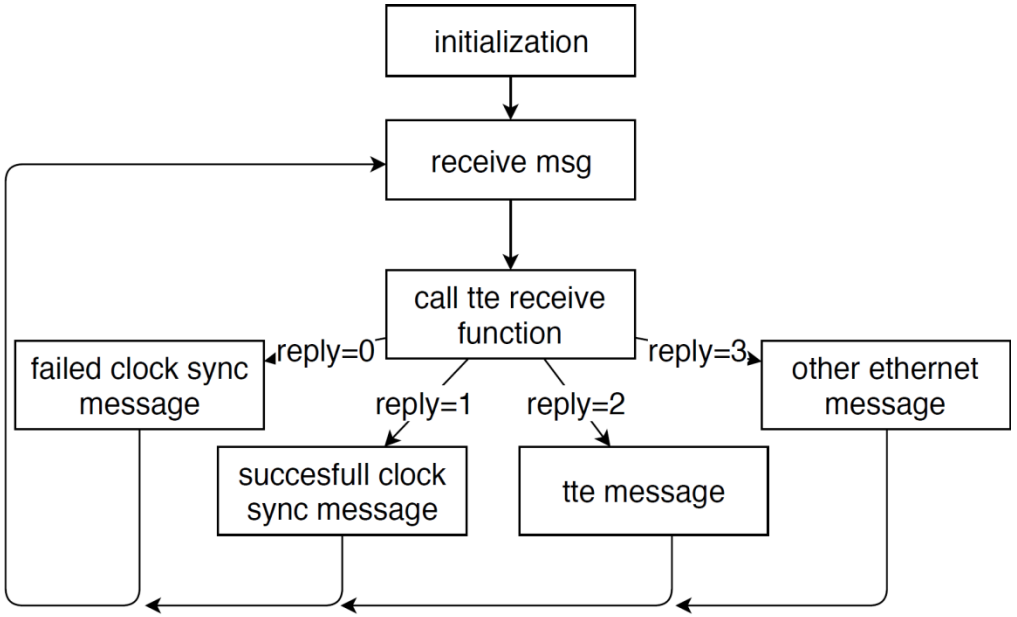
- Based on the Patmos processor (T-CREST platform) and the EthMac controller
  - Open source
  - Software tools for WCET analysis (platin and aiT)



- All the rest is software

Functionality

- Set of functions for sending, receiving, managing
  - **`tte_receive`**
  - **`tte_schedule_send`**
  - **`tte_send_data`**
  - **`handle_integration_frame`**
  - Others…



- Sending according to schedule is managed by the library
  - Data placed in a buffer - send is scheduled
  - Uses timer interrupts

Worst-case execution time

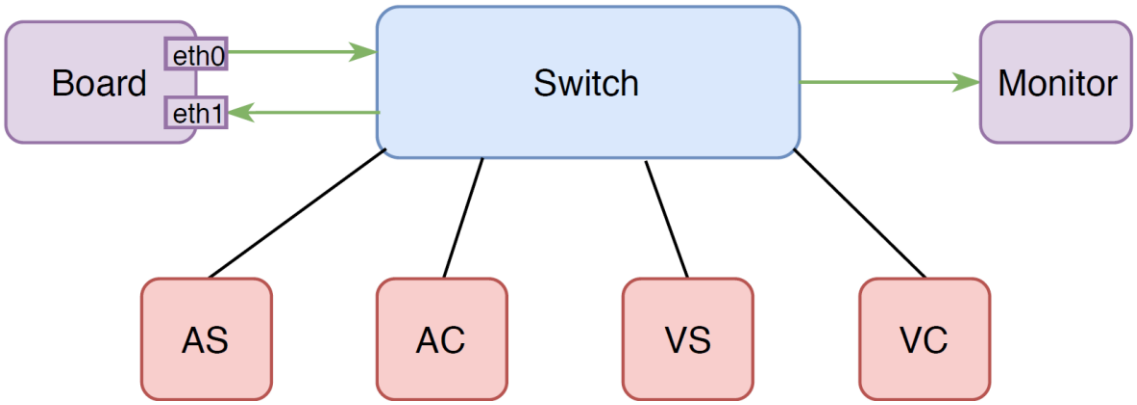
- All functions are analyzable and have bounded WCET

Function	WCET (clock cycles)
tte_clear_free_rx_buffer	10
tte_receive	3028
tte_receive_log	3216
handle_integration_frame	2573
handle_integration_frame_log	2732
tte_prepare_test_data	39138
tte_schedule_send	244
tte_send_data	289
tte_clock_tick	1641
tte_clock_tick_log	1824
tte_code_int	392419
tte_code_tt	40156

Evaluation

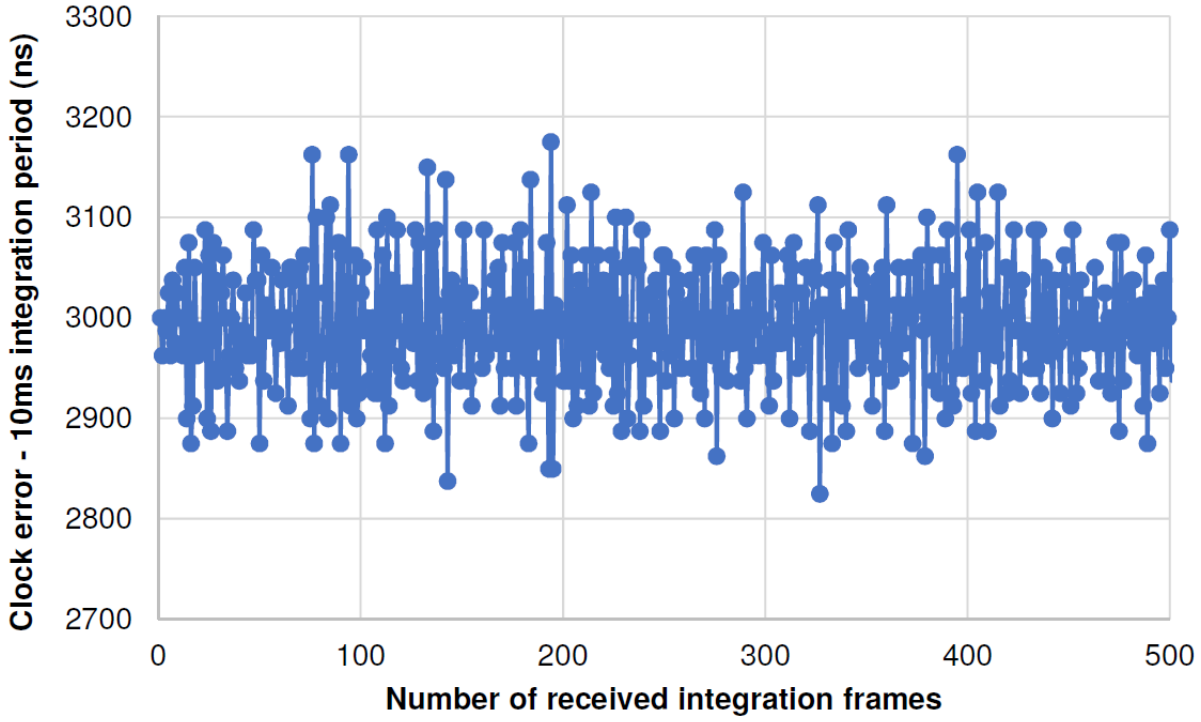
- Our node implemented on FPGA using the Altera DE2-115 board

- Setup for the test
  - TTEthernet switch by TTTech
  - FPGA board implementing our node
  - 4 Linux PC (AS, AC, VS, VC)
  - 1 Monitor Windows PC



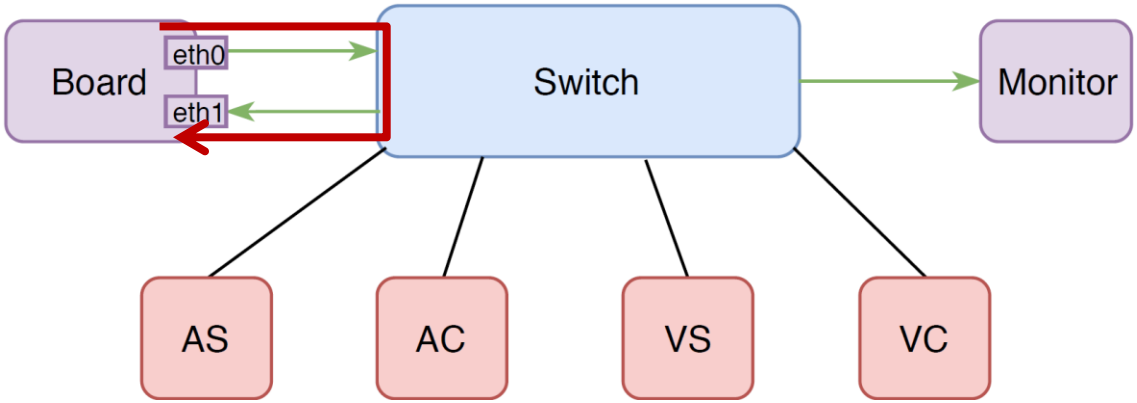
Clock synchronization

- 10ms integration period
- Error ranges between 2787 ns and 3225 ns -> 300ppm clock drift

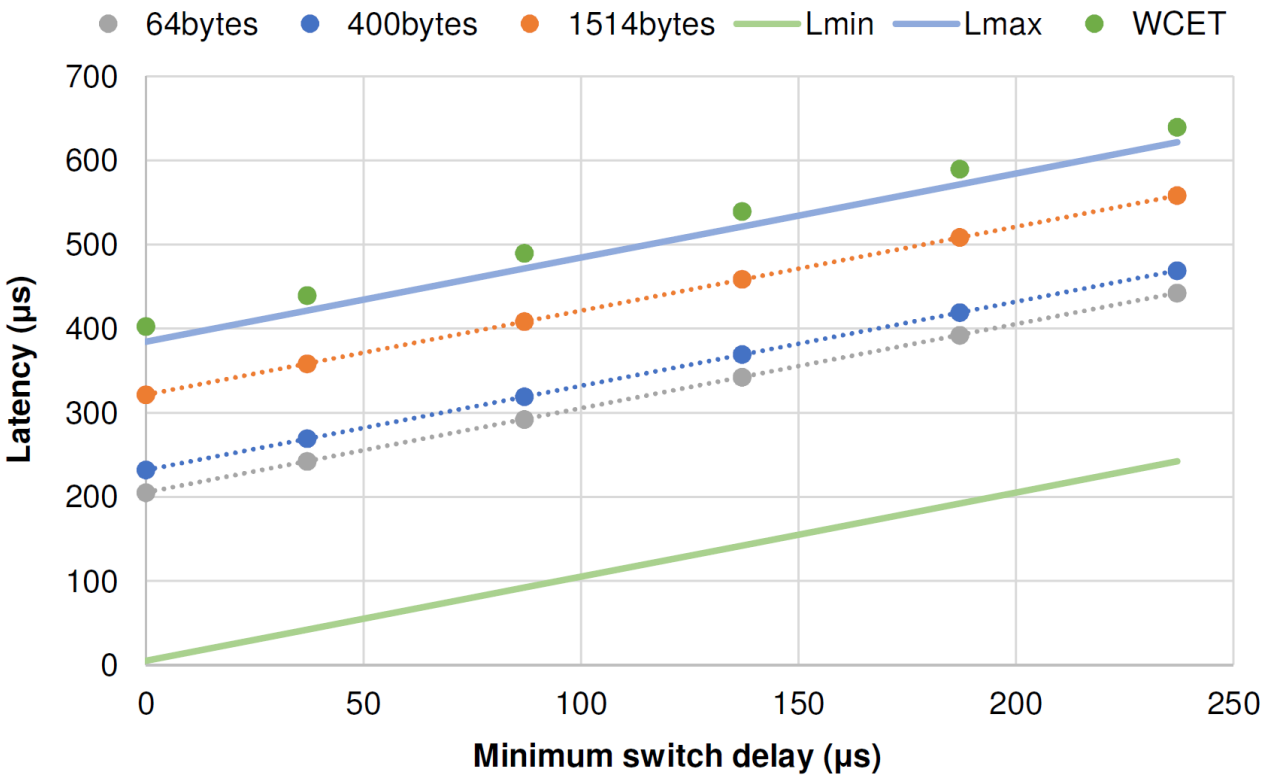


Latency and jitter

- Measuring the loopback latency
  - Duplicated controller
  - Board -> Switch -> Board



Latency and jitter



- Jitter of around 4.6µs

Summary

- TTEthernet node based on the Patmos processor and the EthMac controller
- Time-predictable and fully-analyzable software stack
- Implemented on FPGA and evaluated in real-world setup
- Open-source and no use of proprietary hardware in our node